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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/652,550
Filing Date August 31, 2000
Inventor Keiji Jono et al.
Assignee KMT Semiconductor, LTD
Group Art Unit 2811
Examiner T.F. Tran
Attorney's Docket No. KM1-001
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods
of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods
of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated
Transistor, Trench Isolation Structures Formed in a Semiconductor,
Memory Cells and DRAM

RESPONSE TO NOTICE OF NON-COMPLIANT
AMENDMENT DATED JULY 23, 2002

FAX RECEIVED

AUG 12 2002

T.C. 2800

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.
Tel. 509-624-4276; Fax 509-838-3424
Wells St. John P.S.
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Spokane, WA 99201-3828

Responsive to the Notice of Non-compliant Amendment dated July 23,
2002, Applicant comments as follows:

REMARKS

Applicants state on page 2 of the Response to October 12, 2001 Office
Action, "Please amend the claims as follows:." However, the only
amendments to the claims are cancellation of claims 33-61, no other